Ultra-low-voltage bilayer graphene tunnel FET

Gianluca Fiori, Giuseppe Iannaccone

Dipartimento di Ingegneria dell'Informazione : Elettronica, Informatica, Telecomunicazioni,

Università di Pisa, Via Caruso, 56126 Pisa, Italy.

email : gfiori@mercurio.iet.unipi.it; Tel. +39 050 2217596; Fax : + 39 050 2217522

arXiv:0906.1254v1 [cond-mat.mes-hall] 6 Jun 2009

Abstract

In this work, we propose the Bilayer Graphene Tunnel Field Effect Transistor (BG-TFET) as a device suitable for fabrication and circuit integration with present-day technology. It provides high $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio at ultra-low supply voltage, without the limitations in terms of prohibitive lithography and patterning requirements for circuit integration of graphene nanoribbons. Our investigation is based on the solution of the coupled Poisson and Schrödinger equations in three dimensions, within the Non-Equilibrium Greens (NEGF) formalism on a Tight Binding Hamiltonian. We show that the small achievable gap of only few hundreds meV is still enough for promising TFET operation, providing a large $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio in excess of 10^3 even for a supply voltage of only 0.1 V. Key to this performance is the low quantum capacitance of bilayer graphene, which permits to obtain an extremely small sub-threshold swing S smaller than 20 mV/decade at room temperature.

Keywords: bilayer graphene, NEGF, tunnel FET, low-power device.

I. INTRODUCTION

Very recent theoretical and experimental papers [1], [2], [3], [4] have shown the possibility of inducing an energy gap (E_{gap}) in bilayer graphene by means of an applied electric field perpendicular to the graphene plane. This property could open the possibility of fabricating carbon-based electron devices, for which a semiconducting gap is required, with state-of-the-art lithography. Let us stress that the alternative option of inducing a gap by means of lateral confinement to fabricate graphene nanoribbon Field Effect Transistors (FETs) [5] requires single-atom control and prohibitive lithography to define widths close to 1 nm [6].

Since the largest attainable E_{gap} in bilayer graphene is of few hundreds meV, band-to-band tunneling strongly limits device performance, so that the $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio of the drain current is typically smaller than 10 [7].

One can however turn this limitation into an advantage, fully exploiting band-to-band tunneling instead of avoiding it, like in Tunnel FETs (TFETs), which have been widely investigated in the past through experiments and simulations, considering different channel materials [8], [9], [10].

The main appeal of TFETs is the possibility of obtaining a sub-threshold swing S well below that obtained in conventional FETs, which would in turn allow to strongly reduce the supply voltage for digital logic well below 0.5 V, and consequently the power consumption [8].

In this regard, it has been recently observed [11] that one-dimensional carbon-based devices are more promising than planar silicon devices, because of the small carrier effective mass, that enhances the I_{on} current, and of the small quantum capacitance in the ON state, which guarantees good electrostatic control of the channel through the gate voltage, improving S.

In this letter, we propose the realization of an ultra-low-power Bilayer Graphene TFET (BG-TFET) and investigate its performance by means of numerical simulations based on the self-consistent solution of the 3D Poisson and Schrödinger equations, within the Non-Equilibrium Green's (NEGF), implemented in our open source code NanoTCAD ViDES [12].

We show that a large $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio in excess of 10^3 can be obtained for a voltage V_{DD} of only 0.1 V. The low quantum capacitance of bilayer graphene allows us to grab the advantages provided by one-dimensional carbon channels also with a planar — more easily manufacturable — structure, and to achieve very low S.

II. RESULTS AND DISCUSSION

The Schrödinger equation has been solved within a p_z orbital basis set in the real space, and details can be found in [7], [13].

The device structure is depicted in Fig. 1a. The considered device is a double-gate BG-TFET, driven by two independent gates, biased with V_{top} and V_{bottom}, respectively. The channel length L is 40 nm, and the p^+ and n^+ reservoirs are 40 nm long and doped with molar fraction f. The bilayer graphene is embedded in an SiO$_2$ dielectric, 3 nm-thick, with relative dielectric constant ε_r=3.9. A gate overlap has also been taken into account, whose effects will be discussed later on.

In Fig. 1a a band edge profile of the TFET in the OFF state is also shown. Since the potential in the vertical direction falls linearly, the device is in the OFF state (minimum current in the channel) for $V_{\mathrm{bottom}} = V_{\mathrm{min}} \equiv (V_{\mathrm{top}} - V_{\mathrm{bottom}})/2 + V_{\mathrm{DS}}/2$, where V_{DS} is the drain-to-source voltage.

The conduction and valence bands can be divided in five sub-regions along the transport direction: the source, the so-called virtual source, the channel, the virtual drain and the drain. Deep in the source and drain regions the conduction and the valence bands coincide because the vertical electric field rapidly goes to zero. A gap is induced in all the regions surrounded by the top and the bottom gates, where a differential voltage $V_{\mathrm{diff}} \equiv V_{\mathrm{top}} - V_{\mathrm{bottom}}$ is imposed, i.e. in the virtual source and drain regions and in the channel.

Six different fluxes of carriers contribute to transport, identified with a letter in Fig. 1a: tunneling electrons (A and B fluxes), tunneling holes (E and D fluxes) and thermally emitted electrons (C) and holes (F). In order to obtain a small I_{off}, all mentioned fluxes have to be minimized through proper band engineering.

One solution could be inducing a large energy gap, which translates in imposing a large vertical electric field. This option is however limited by the breakdown field of the oxide, and by the gate leakage current. To this purpose, we have chosen SiO_2 as a gate dielectric, which guarantees an intrinsic breakdown field close to 14 MV/cm [14] (well above the simulated vertical electric fields), and a large graphene/SiO_2 band offset (larger than 3 eV), which ensures very small gate leakage currents.

The molar fraction of the source and drain leads instead determines E_1 and E_2, the difference between the mid-gap potential in the channel (E_{ref}) and the mid-gap in the virtual drain and in the drain, respectively (same considerations obviously follow for the source): the higher f, the higher E_1 and E_2. Decreasing E_1 and E_2 can help in reducing E and D (or A and B in the source), but in turns increases of thermionic emission (C and F).

Let us focus on the performance of the BG-TFET with ultra-low supply voltage V_{DD}=0.1 V. In Fig. 1b we show the transfer characteristics as a function of V_{bottom} of a device with molar fraction $f = 2.5 \times 10^{-3}$, for fixed differential gate voltages V_{diff} =6, 6.5, 7 and 8 V.

As can be noted, differently from what happens in double gate BG-FETs [7], the BG-TFET can be perfectly switched off, with a steep sub-threshold behavior (always smaller than 20 mV/dec) and a large $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio also for a very low V_{DD} (e.g. $I_{\mathrm{on}}/I_{\mathrm{off}}$=4888 for V_{diff}=8 V).

Due to the large vertical electric field, particular attention has also to be posed on the gate leakage current. We can estimate its value using a well-tested analytical model for Si-SiO_2 gate stacks based on WKB approximation of the triangular barrier [15]. We find that the gate current is of the order of 10^{-6} μA/μm for $V_{\mathrm{diff}} = 7$ V, and 10^{-4} μA/μm for $V_{\mathrm{diff}} = 8$ V, i.e. negligible with respect to the smallest drain currents considered in our simulations.

In Fig. 2a we show the transfer characteristics as a function of V_{bottom}, for V_{diff}=7 V, and for different dopant molar fractions f in the drain and source leads. As f is increased, the $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio degrades, since I_{off} increases, while I_{on} remains almost constant.

In Fig. 2b, we show the transfer characteristics as a function of gate overlap. As can be seen, the smaller the overlap, the higher the I_{off} current, since it is the energy gap of the virtual reservoirs that suppresses tunneling from contacts to the channel.

In order to investigate the performance of single-gate devices, we have also performed simulations of a device with asymmetric gate oxide thicknesses (Fig. 2c): top oxide is 3 nm, and the bottom oxide is 9 nm. In this case the bottom gate voltage is kept at a constant bias of -12 V, whereas the top gate is used as the control gate.

As can be noted, an $I_{\text{on}}/I_{\text{off}}$ ratio of few hundreds can be still obtained. The sub-threshold swing (and then the $I_{\text{on}}/I_{\text{off}}$ ratio) can be improved with a thicker bottom oxide of the order of 100 nm, that would reduce the capacitive coupling between channel and bottom gate. We however limited our analysis to 9 nm, because of numerical convergence problems encountered when dealing with larger structures.

As noted in Ref. [11], one-dimensional channels are typically more appealing for tunneling device applications than planar two-dimensional channels, since their quantum capacitance C_Q is smaller than the electrostatic capacitance C_{ox} even in the ON state. Such condition guarantees a good gate control over the potential barrier and larger $I_{\text{on}}/I_{\text{off}}$.

In Fig. 3a, we show ϕ_C, the electrostatic potential in the middle of the channel, as a function of the bottom gate voltage, for $f = 2.5 \times 10^{-3}$ and $V_{\text{diff}} = 7$ V. On the same plot, we also show the line $\phi_C = V_{\text{bottom}} - V_{\text{min}} + V_{\text{DS}}/2$, corresponding to ideal control of the channel potential from the gate voltage. As can be seen, also for larger gate voltages, ϕ_C reasonably follows V_{bottom}, and no channel potential saturation is observed. As indeed shown in Fig. 3b, where the ratio C_Q/C_{ox} is depicted, for small voltages the device is working in the Quantum Capacitance Limit (i.e. $C_Q \ll C_{\text{ox}}$), whereas for larger values C_Q is comparable with C_{ox}. However, it never reaches the condition $C_Q \gg C_{\text{ox}}$ as in silicon TFETs. As a consequence, despite its bidimensionality, bilayer graphene is appealing for tunneling devices applications.

III. Conclusion

In conclusions, we have performed a numerical analysis of a bilayer graphene tunnel field effect transistors, based on the self-consistent solution of the 3D Poisson/Schrödinger equations, within the NEGF formalism. Large $I_{\text{on}}/I_{\text{off}}$ ratios can be obtained even for an ultra-low supply voltage of only 100 mV, thanks to an extremely steep sub-threshold slope. The low quantum capacitance of bilayer graphene allows the BG-TFET to have most of the advantages of one-dimensional TFETs, but none of the disadvantages in terms of structure patterning and lithography. Indeed, since present-day lithography is adequate for the fabrication of BG-TFETs, and the single-gate driving option with constant bottom gate bias is suitable for planar integration, we consider the device very promising for fabrication experiments and circuit integration.
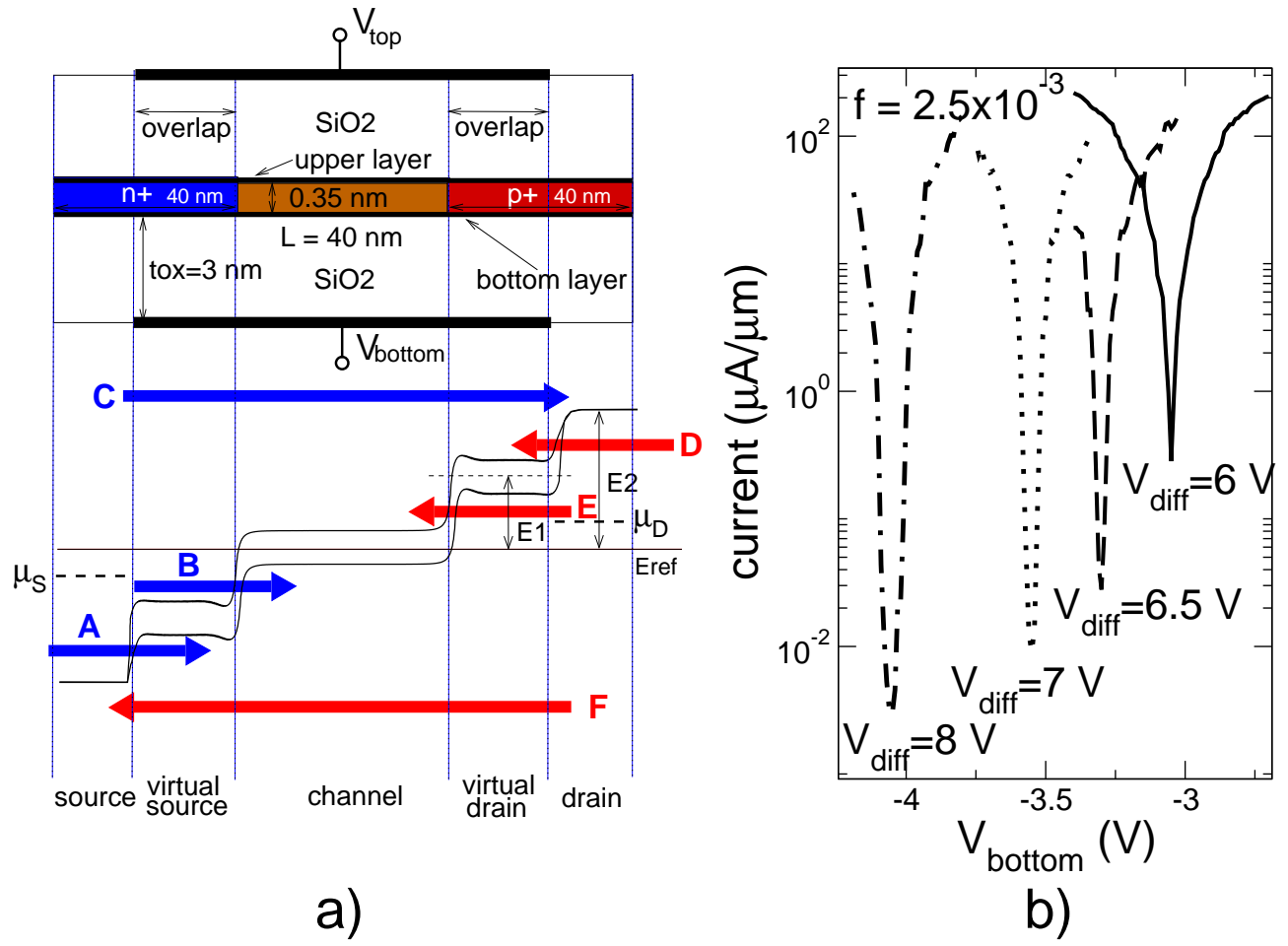
REFERENCES

[1] E. McCann and V.I. Falko, "Landau-level degeneracy and quantum hall effect in a graphite bilayer", *Phys. Rev.Lett*, vol. 96, pp. 086805–, 2006.

[2] J. Nilsson, A.H. Castro Neto, F. Guinea, and N.M.R. Peres, "Electronic properties of graphene multilayers", *Phys. Rev. Lett.*, vol. 97, pp. 266801–, 2006.

[3] T. Ohta, A. Bostwick, T. Seyller, K. Horn, and E. Rotenberg, "Biased bilayer graphene: Semiconductor with a gap tunable by the electric field effect", *Science*, vol. 313, pp. 951–954, 2006.

[4] V. Ryzhii, M. Ryzhii, A. Satou, T. Otsuji, and N. Kirova, "Device model for graphene bilayer field-effect transistor", *http://arXiv:0812.4490*, vol. -, pp. –, 2008.

[5] Z.Chen, Y-M. Lin, M. J. Rooks, and P. Avouris, "Graphene nano-ribbon electronics", *Phys. E*, vol. 40, pp. 228–232, 2007.

[6] G. Fiori and G. Iannaccone, "Simulation of graphene nanoribbon field-effect transistors", *IEEE Electr. Dev. Lett.*, vol. 28, pp. 760–762, 2007.

[7] G. Fiori and G. Iannaccone, "On the possibility of tunable-gap bilayer graphene", *IEEE Electr. Dev. Lett.*, vol. 30, pp. 261–264, 2009.

[8] W. Hansch, C. Fink, K. Schulze, and I. Eisele, "A vertical mos-gated esaki tunneling transistor in silicon", *Thin Solid Films*, vol. 369, pp. 387–389, 2000.

[9] S.O. Koswatta, M.S. Lundstrom, and D.E. Nikonov, "Influence of phonon scattering on the performance of p-i-n band-to-band tunneling transistors", *App. Phys. Lett.*, vol. 92, pp. 043125–, 2008.

[10] P. Zhao, J. Chauhan, and J. Guo, "Computational study of tunneling transistor based on graphene nanoribbon", *Nano Lett.*, vol. 9, pp. 684–688, 2009.

[11] J. Knoch and J. Appenzeller, "Tunneling phenomena in carbin nanotubes field-effect transistors", *Phys. Stat. Sol.*, vol. 205, pp. 679–694, 2008.

[12] "Available at: http://www.nanohub.org/tools/vides".

[13] G.Fiori and G.Iannaccone, "Performance analysis of graphene bilayer transistors through tight-binding simulations", *to appear in the Proceedings of International Workshop of Computational Electronics 2009*, vol. -, pp. –, 2009.

[14] A. Campera, G. Iannaccone, and F. Crupi, "Modeling of tunnelling currents in hf-based gate stacks as a function of temperature and extraction of material parameters", *IEEE Trans. Electron Devices*, vol. 54, pp. 83–89, 2007.

[15] M. Depas, B. Vermeire, P.W. Mertens, R.L. Van Meirhaeghe, and M.M. Heyns, "Determination of tunneling parameters in ultra-thin oxide layer poly-si/sio$_2$/si structure", *Solid State Electr.*, vol. 38, pp. 1465–1471, 1995.

Fig. 1.   a) Sketch of the double-gate bilayer graphene TFET: the channel length is 40 nm, and n$^+$ and p$^+$ reservoirs are 40 nm long with molar fraction f. The device is embedded in 3 nm-thick SiO$_2$ dielectric. V_{top} and V_{bottom} are the voltages applied the top and bottom gate, respectively. Gate overlap has been also considered. Below, band edge profile of the device in the OFF state; b) Transfer characteristics of the double-gate BG-TFET for different V_{diff}. f is equal to 2.5×10^{-3} and $V_{\text{DS}} = 0.1$ V.

Fig. 2.   a) Transfer characteristics of TBG-FETs for V_{diff}=7 V, $V_{\text{DS}} = 0.1$ V, and different molar fractions f. V_{min}=-3.55 V; b) Transfer characteristics of BG-TFET for V_{diff}=7 V, $V_{\text{DS}} = 0.1$ V, and different gate overlap. V_{min}=-3.55 V. c) Transfer characteristic for a device with asymmetric oxide thicknesses: the top oxide thickness is 3 nm, and the bottom oxide thickness is 9 nm. V_{bottom} is fixed to -12 V and $V_{\text{DS}} = 0.1$ V.

Fig. 3.   a) electrostatic potential in the middle of the channel ϕ_C as a function of the bottom gate voltage (solid line). The dashed line refers the case in which the gate control is ideal, i.e. $\phi_c = (V_{\text{bottom}} - V_{\text{min}}) + V_{\text{DS}}/2$. In the inset the equivalent capacitance circuit of the device is shown; b) ratio of the quantum capacitance C_Q and the oxide capacitance C_{ox}.
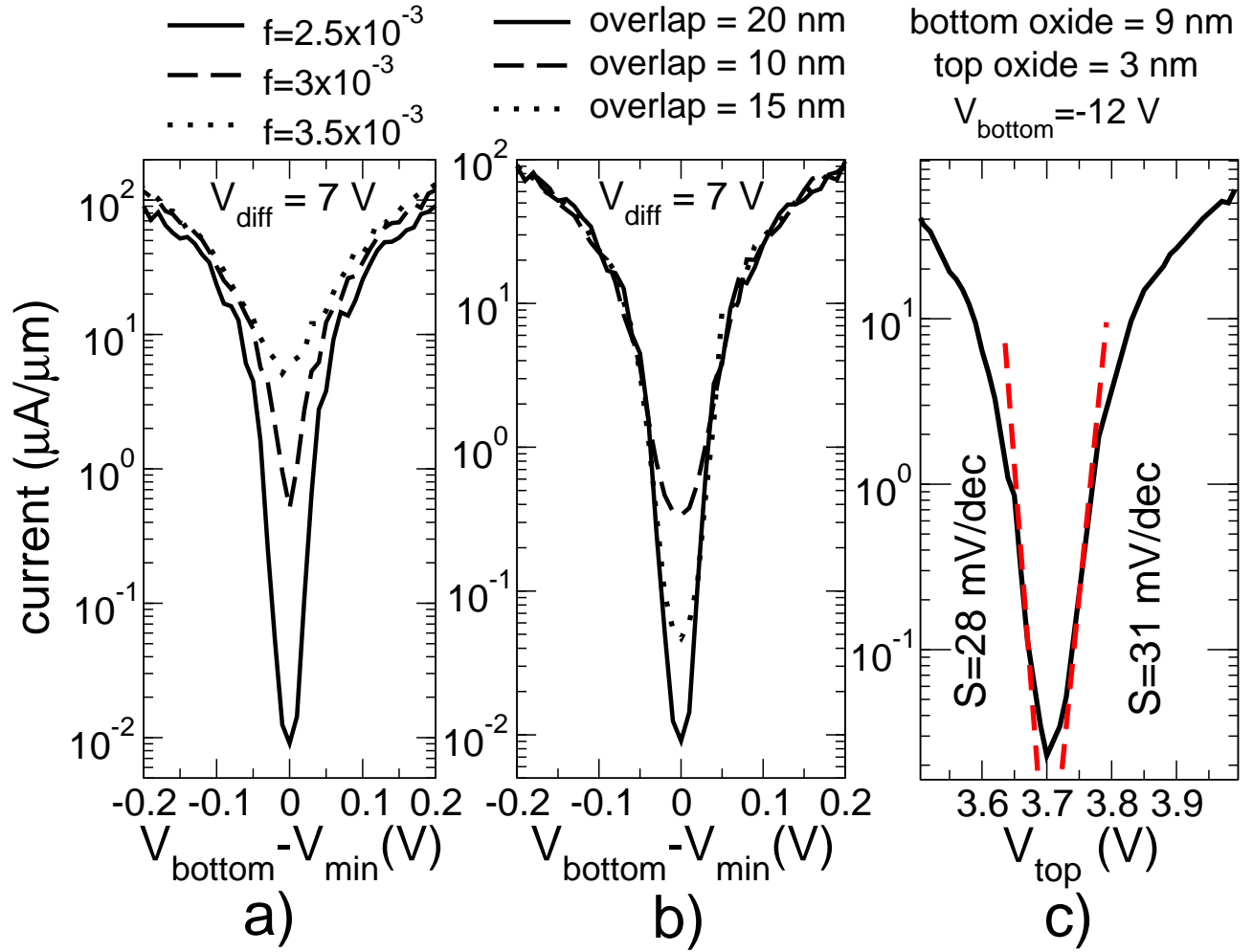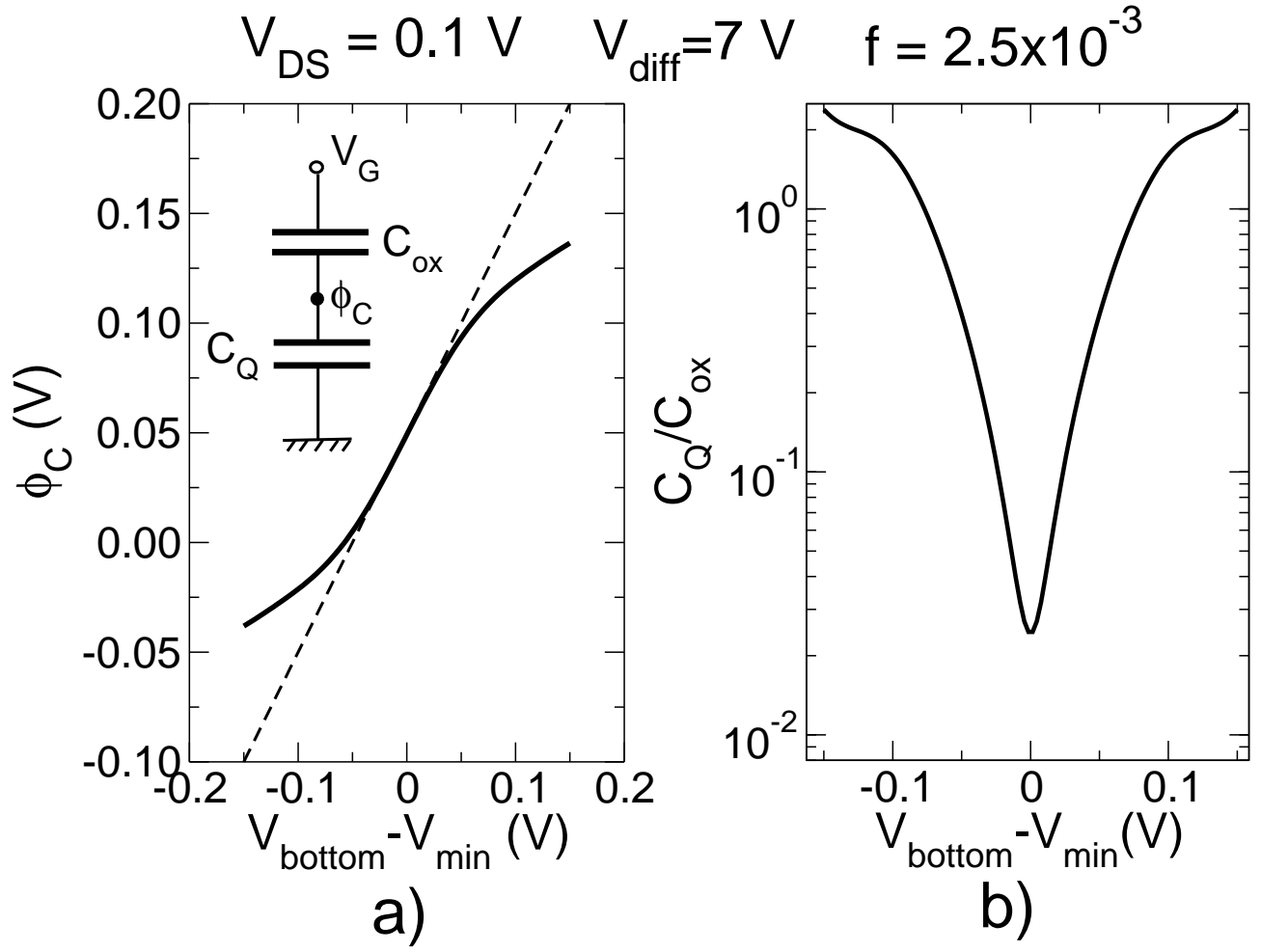
FIG. 1

FIG. 2

$V_{DS} = 0.1$ V $V_{diff} = 7$ V $f = 2.5 \times 10^{-3}$

a)

b)

FIG. 3